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(58) Field of search
H4T

(54) Video signal manipulation system

(57) A video signal manipulation system has a character/graphics generator (10) and a video memory (30) for storing data provided thereby. A manipulation memory (33) holds selected address parameters pertaining to individual displayed video lines defining the start addresses of picture information read out from the video memory (31). Means (32) is provided for incrementing or decrementing video memory addresses commencing from the start address available from the manipulation memory (33) to allow data from the video memory (30) to be read out in a manipulated sequence. Effects such as scrolling, wipes and inversion of the picture are possible. The start addresses may be updated during the frame blanking period.

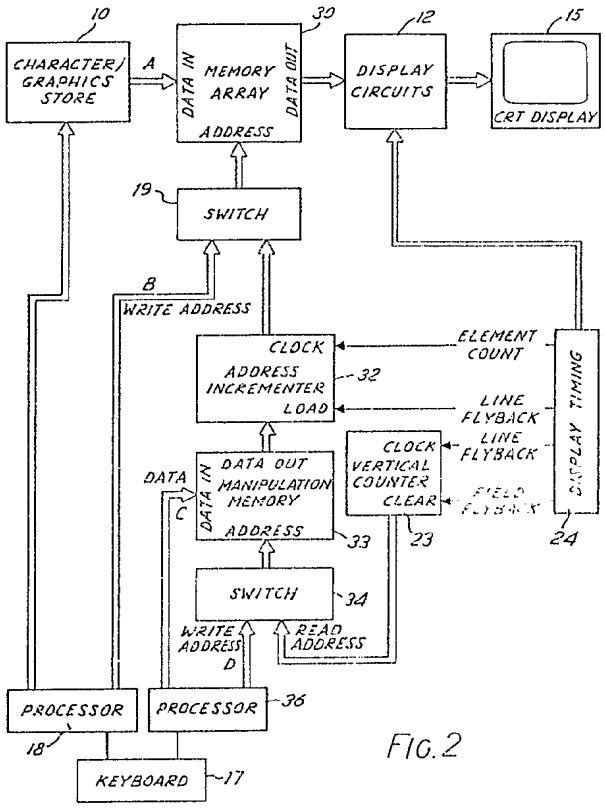

FIG. 2

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The drawing(s) originally filed was (were) informal and the print here reproduced is taken from a later filed formal copy.

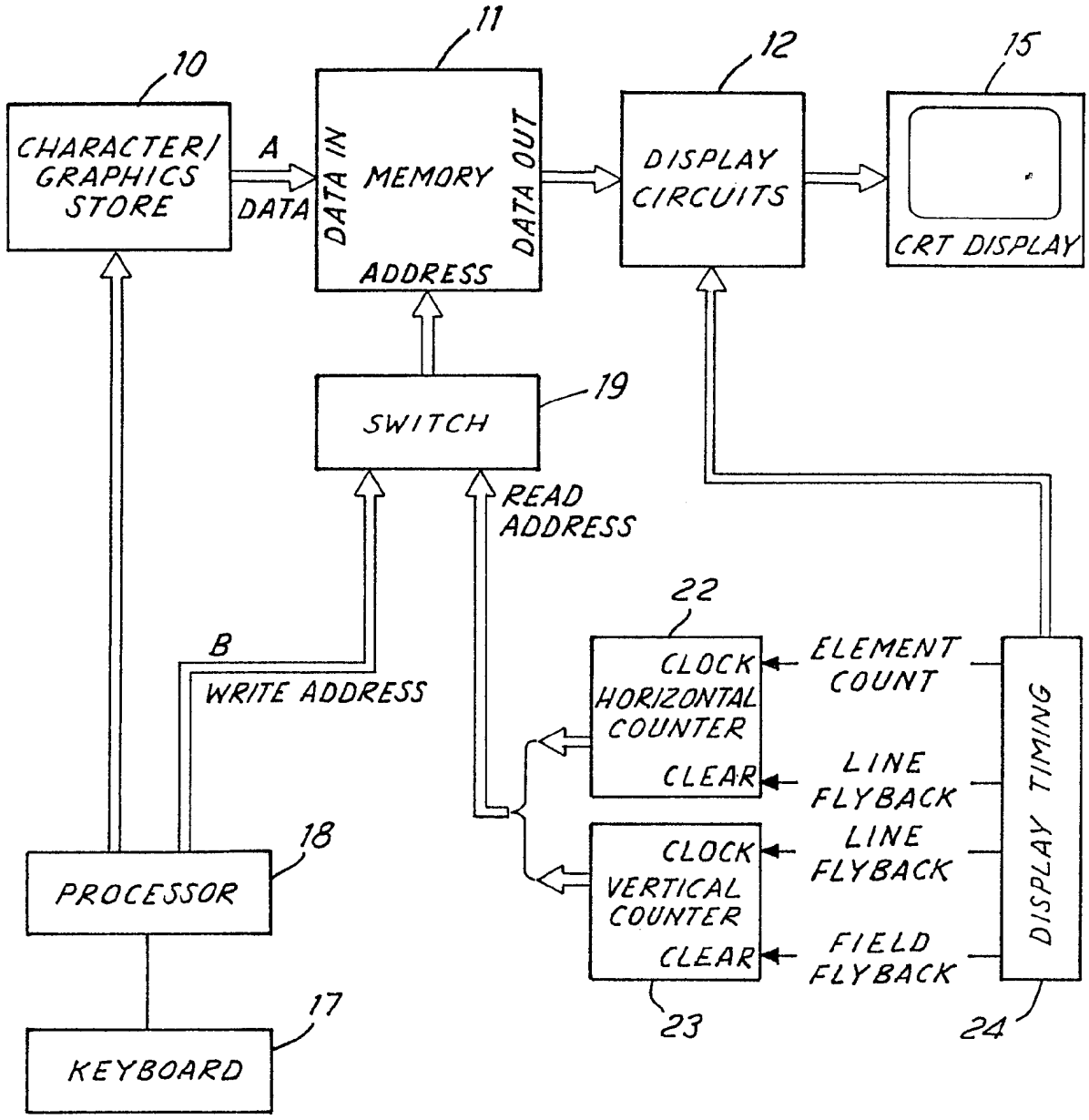
10
CHARACTER/ GRAPHICS STORE
A
DATA
11
DATA IN
MEMORY
ADDRESS
DATA OUT
12
DISPLAY CIRCUITS
15
CRT DISPLAY
19
SWITCH
READ ADDRESS
B
WRITE ADDRESS
22
CLOCK HORIZONTAL COUNTER
CLEAR
ELEMENT COUNT
LINE FLYBACK
CLOCK VERTICAL COUNTER
CLEAR
LINE FLYBACK
FIELD FLYBACK
DISPLAY TIMING
18
PROCESSOR
17
KEYBOARD
23
24

FIG.1

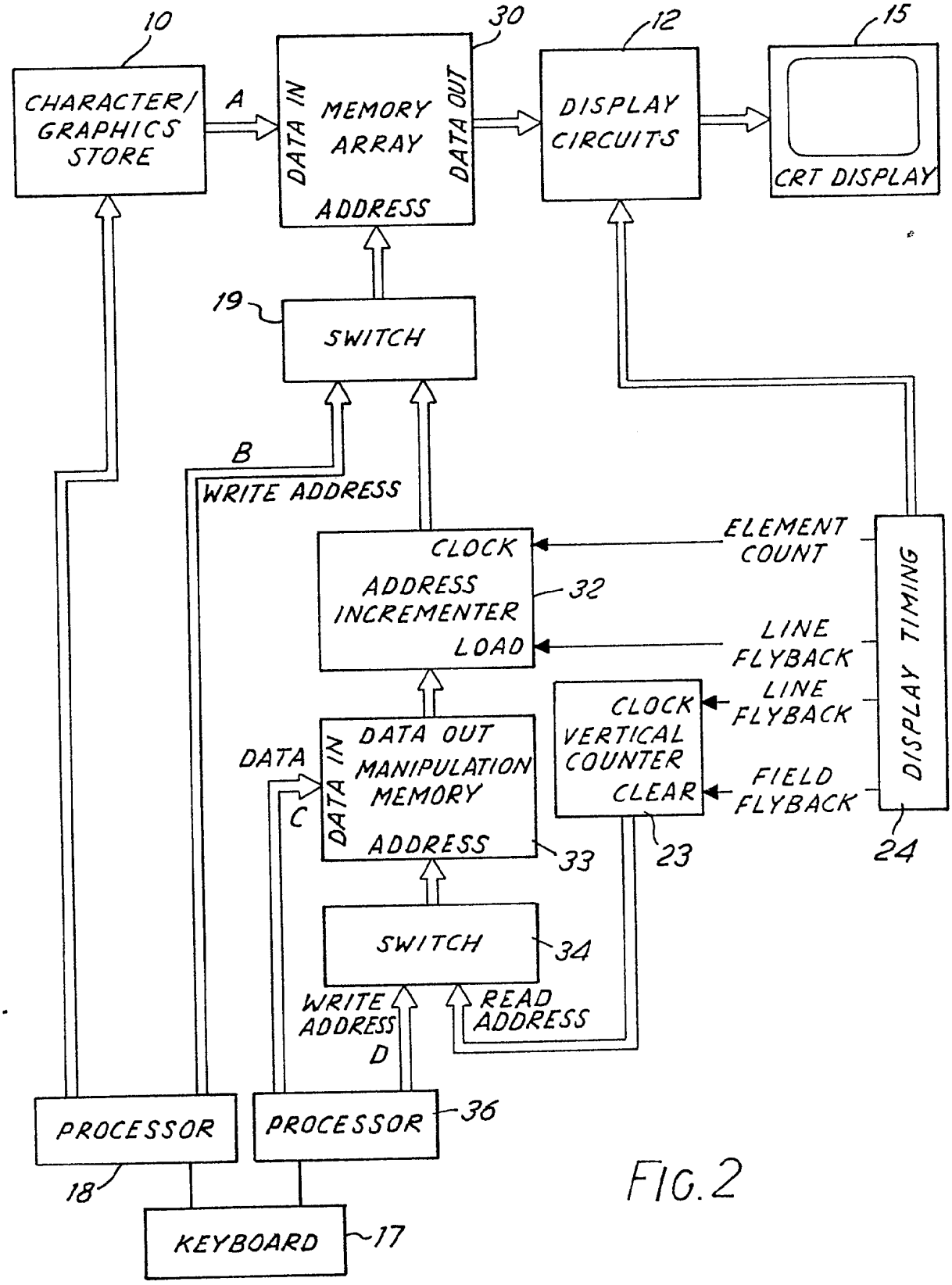
10
CHARACTER/ GRAPHICS STORE
A
30
DATA IN
MEMORY ARRAY
DATA OUT
ADDRESS
12
DISPLAY CIRCUITS
15
CRT DISPLAY
19
SWITCH
B
WRITE ADDRESS
CLOCK
ADDRESS INCREMENTER
32
LOAD
ELEMENT COUNT
LINE FLYBACK
DISPLAY TIMING
CLOCK
VERTICAL COUNTER
CLEAR
LINE FLYBACK
FIELD FLYBACK
24
23
DATA
C
DATA IN
DATA OUT
MANIPULATION MEMORY
ADDRESS
33
SWITCH
34
WRITE ADDRESS
D
READ ADDRESS
PROCESSOR
18
PROCESSOR
36
KEYBOARD
17

FIG. 2

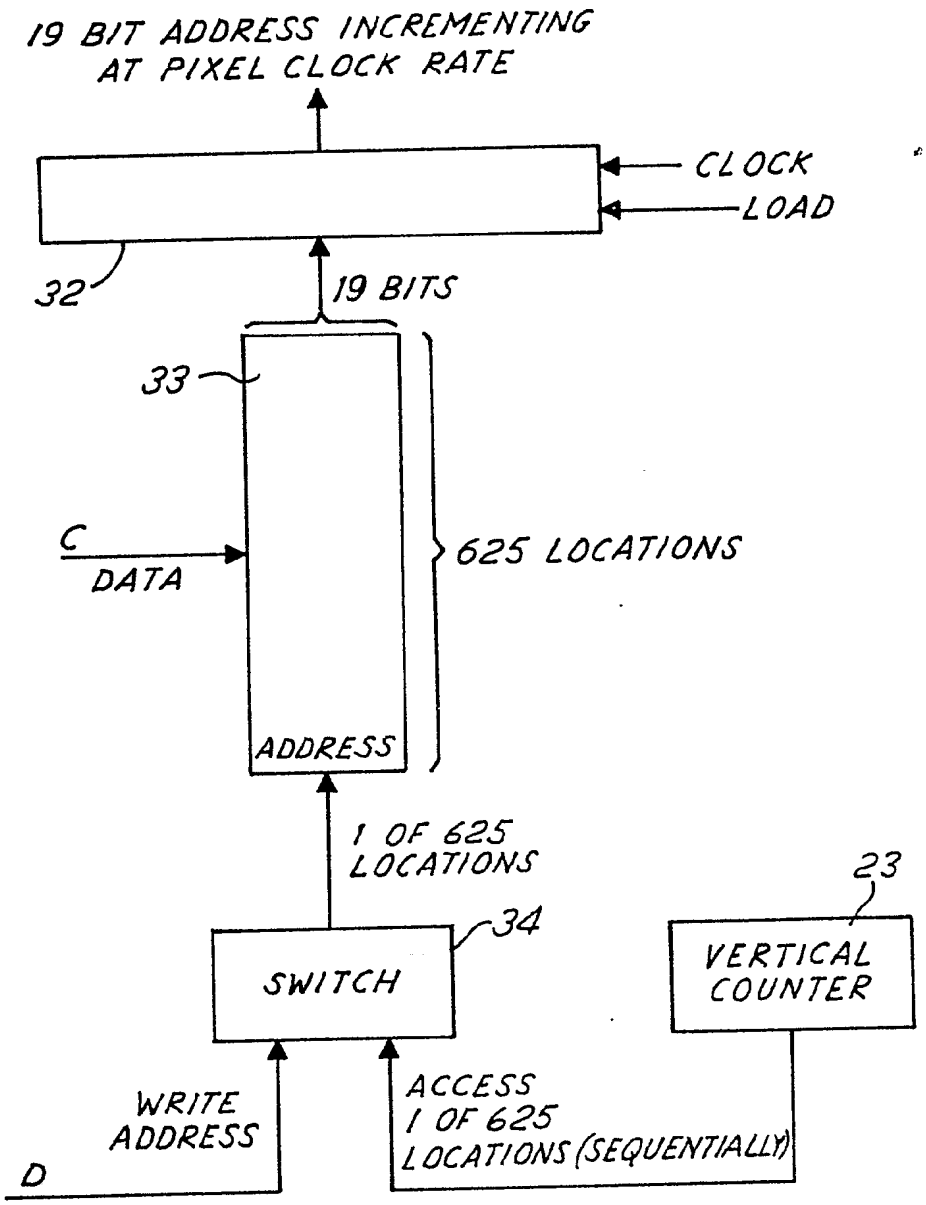
19 BIT ADDRESS INCREMENTING AT PIXEL CLOCK RATE
CLOCK
LOAD
32
19 BITS
33
C
DATA
625 LOCATIONS
ADDRESS
1 OF 625 LOCATIONS
23
34
SWITCH
VERTICAL COUNTER
WRITE ADDRESS
D
ACCESS 1 OF 625 LOCATIONS (SEQUENTIALLY)

FIG. 3

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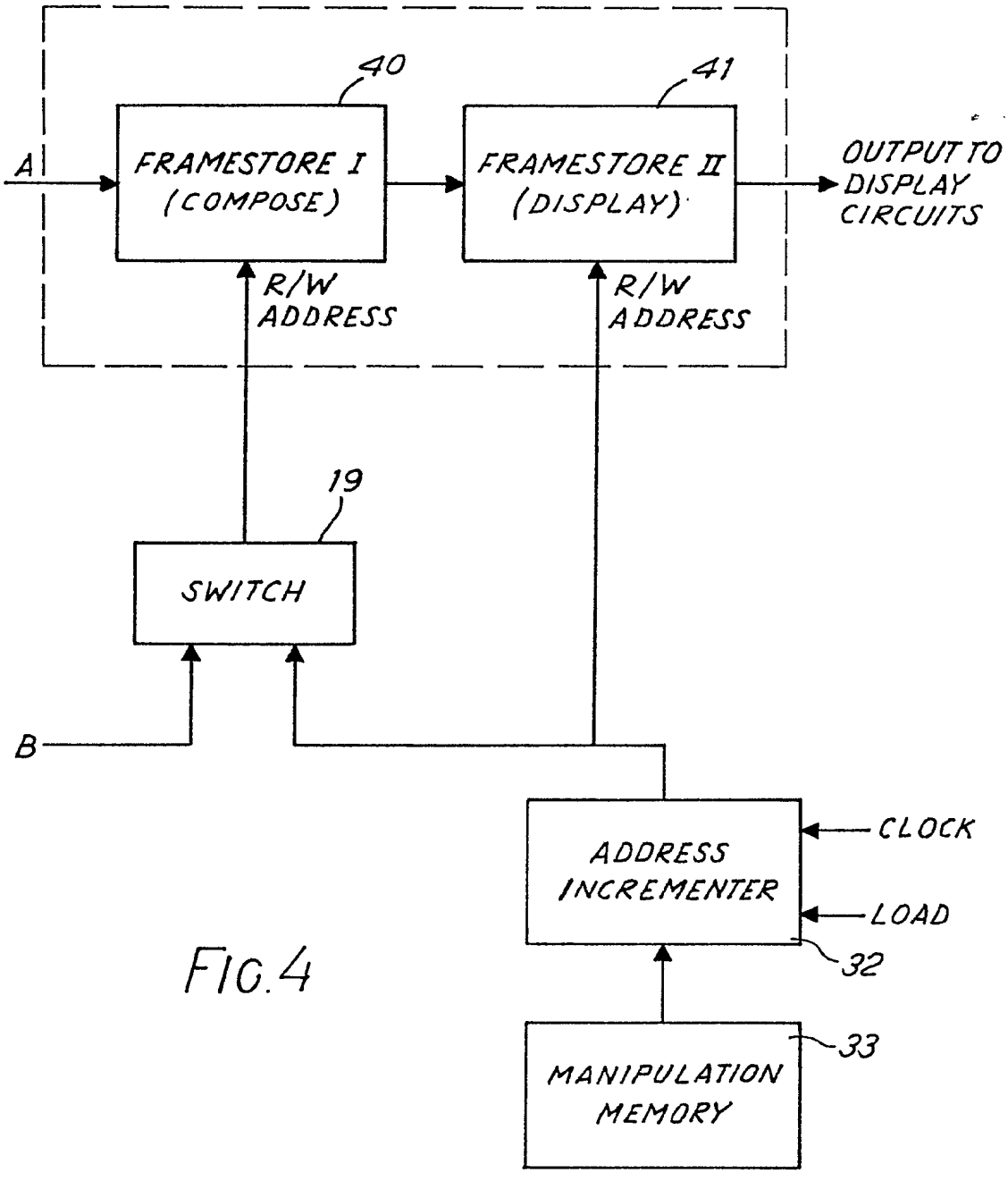

FIG. 4

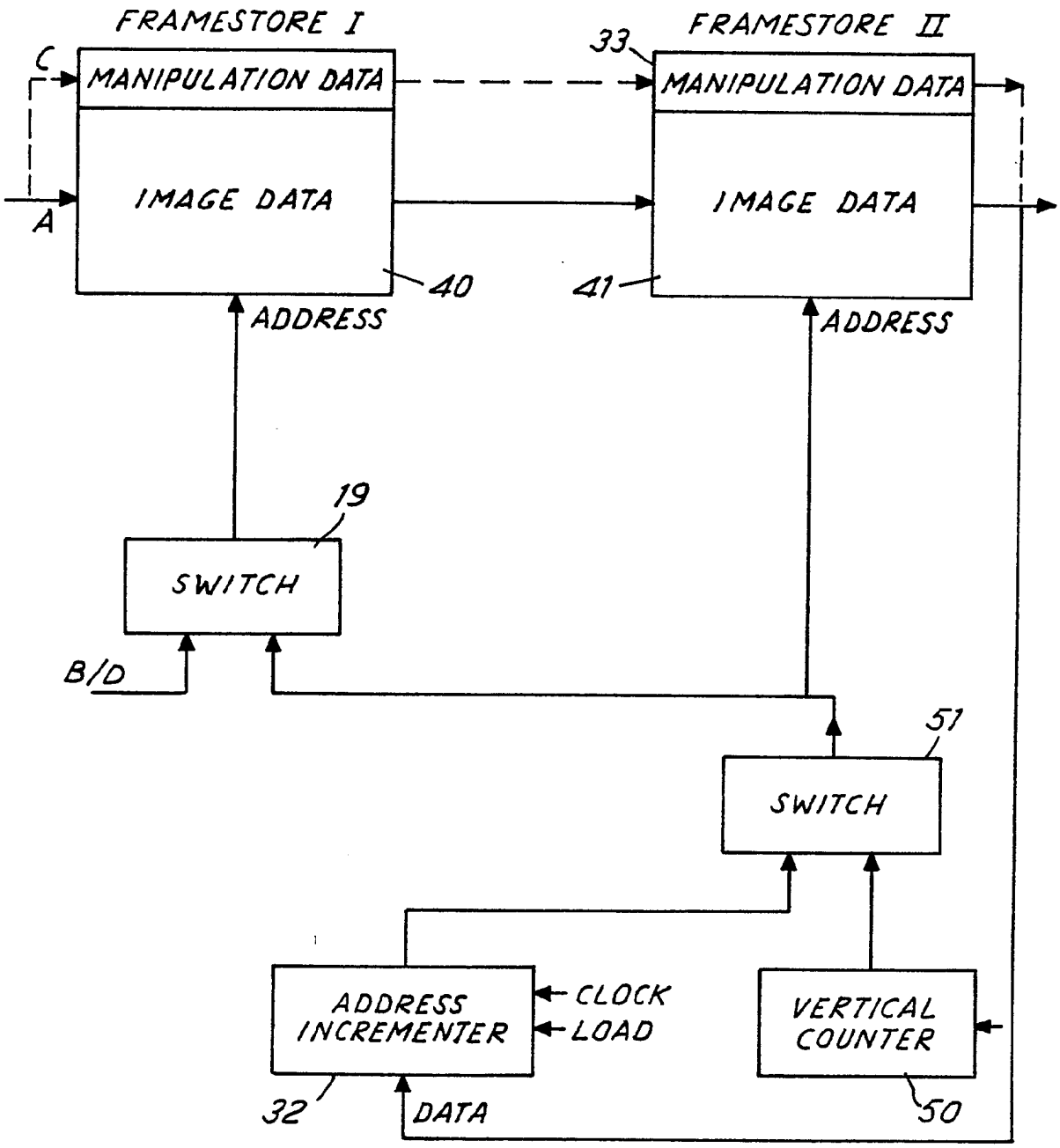
FRAMESTORE I
FRAMESTORE II
33
C
MANIPULATION DATA
MANIPULATION DATA
IMAGE DATA
IMAGE DATA
A
40
41
ADDRESS
ADDRESS
19
SWITCH
B/D
51
SWITCH
ADDRESS INCREMENTER
CLOCK
LOAD
VERTICAL COUNTER
32
DATA
50

FIG. 5

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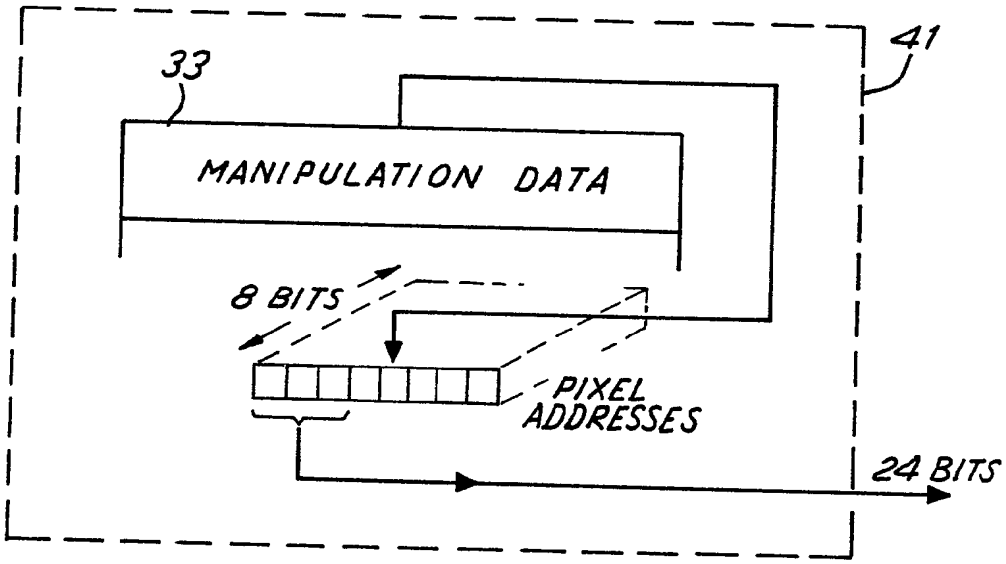

FIG. 6

SPECIFICATION

Manipulation system

The invention relates to a character/graphics manipulation system.

With the proliferation of micro-processors in recent years numerous applications have arisen for the display of graphics and alpha-numeric information on a cathode ray tube display. Applications include graphics displays for industrial process control, broadcast television and the use of visual display units for communicating with micro-processors and computers.

Almost all cathode ray tube displays use a raster scanning technique for displaying pictures in which a spot of light, whose intensity is modulated by the picture information, starts in the top left hand corner of the tube and scans horizontal lines from left to right progressively down the screen. Graphics and alpha-numeric information is commonly presented on such a display by dividing the picture area into rows and columns to form a rectangular matrix of rectangular elements. In the case of simple alpha numeric displays each element forms a discrete character or symbol. In the case of more complicated graphics displays each element represents a small rectangle whose hue and brightness is individually defined such that the rectangular matrix forms a high resolution display or picture. In this case each element is known as a pixel and typically 500,000 such elements must be specified to form a display (e.g. 700 x 576 pixels).

A typical known static display system is shown in Figure 1.

Details of each character or pixel in the rectangular matrix are stored in a memory 11, typically comprising a digital frame store. This memory is filled from a computer or other picture source; in this case from a character/graphics store 10. Addressing of the frame store memory 11 may be taken from one of two sources via a switch 19. When a picture or display is to be input to the framestore the address of the memory is supplied from the computer, represented by the processor 18 and associated keyboard 17. When the picture is being read out for display however, the address of the memory is supplied by counters 22, and 23 under the control of timing block 24. The picture read out for display is converted into suitable format by internal registers and a Digital-to-Analogue Converter (DAC) within block 12 before receipt by display 15.

The timing circuits 24 provide the line, field and frame waveforms required to generate the cathode ray tube raster and include an oscillator locked to the t.v. line waveform to define the horizontal width of each character or pixel and this is provided by the element count from timer 24. The two counters 22, 23 divide the display into a rectangular matrix of elements. The horizontal counter 22 defines the number of elements on each t.v. line and the vertical counter 23 defines the number of raster lines which form the display.

Typically the characters, typed on the keyboard, are accessed from the store 10 for entry into the desired write address of the memory 11. This address can be chosen using a moveable screen cursor under keyboard control in well known manner. The read side of the memory works in an entirely sequential address accessing manner on a repetitive basis under block 24 control. Hence character or graphics entries are slowly built up by the operator whilst monitoring the results on the display 15.

Although the Figure 1 arrangement is adequate for display systems where the graphics or alpha-numeric display is static, when movement of the display is required, problems would arise. In the case of the pixel based display described, over 500 thousand locations could be present in the memory 11. To attempt movement of a graphics image around the screen with the system shown would require a constant updating of many if not all locations via the keyboard control, clearly a very slow process, and not assisted by the relatively slow operational rate of the processor 18 relative to normal video rates.

Although some special effects devices in broadcast television are available for dynamic effects, because of their prohibitive cost and complexity requirement to enable real time operation to be achieved, they do not lend themselves for use as a graphics or character display system.

The present invention is concerned with providing a cost effective yet versatile system for graphics use.

According to the invention there is provided a manipulation system comprising a character/graphics generator, a video memory for storing data provided by the character/graphics generator, a manipulation memory for holding selected address parameters pertaining to individual displayed video lines defining the start addresses of picture information read out from the video memory and means for incrementing or decrementing video memory addresses commencing from the start address available from the manipulation memory to allow data from the video memory to be read out in a manipulated sequence.

The video memory may comprise first and second video stores for storing data indirectly and/or directly provided by the character/graphics generator.

The system may be configured to allow only the first video memory to receive character/graphics data from the generator and thereafter to rapidly transfer the composed image to the second video memory for display.

The manipulation memory may form part of the video memory.

In order that the invention and its various other preferred features may be understood more easily, some embodiments thereof will now be described, by way of example only, with reference to the accompanying drawings in which:

Figure 1 shows a known display system capable of providing static displays;

Figure 2 shows an embodiment of the invention capable of dynamic effects;

Figure 3 shows further details of an address manipulation mechanism employed in the embodiment of Figure 2;

Figure 4 shows in more detail an image storage configuration employed in the embodiment of Figure 2;

Figure 5 shows a modified image and manipulation storage configuration usable in the embodiment of Figure 2; and

Figure 6 shows the accessing of the manipulation memory of Figure 5 in more detail.

The Figure 2 arrangement provides a relatively inexpensive configuration capable of achieving a number of dynamic effects.

The characters generated from store 10 are received by memory array 30. For reasons discussed below, in practice two memories are present within array 30, but for ease of understanding they will be considered here as a single memory. The transfer of character/graphics is under the control of the keyboard 17 and processor 18. Switch 19 as before allows the designated write addresses to be accessed in the memory 30. Read out of the image for display is now under the influence of a manipulation memory 33 and address incrementer 32. Memory 33 can be provided with a number of storage locations, e.g. 625, equivalent to the number of t.v. lines of display. Each location in memory 33 is provided with a pixel address decided by the operator using keyboard 17 and processor 36, as is the write address for memory 33 provided via switch 34. To read out the image data from memory array 30 for display, each address in manipulation memory 33 is sequentially accessed at line rate (determined by vertical counter 23) so that for the start of any given display line, the pixel address for that line will be read out from memory 33 into address incrementer 32. This pixel address is the initial address accessed in memory array 30 during that line period, thereafter sequential addresses are accessed at pixel rate due to the pixel (element count) clock from timing block 24 incrementing the initially entered address each time this clock pulse is received. Approximately 700 pixel addresses are accessed during this line period for a typical television display. At the end of the line period a new address is entered into incrementer 32 from memory 33 and the read operation for the pertinent addresses within array 30 is effected during the next line period.

Although processor 36 is shown separate to processor 18, in practice they could share functions and be fabricated from standard microprocessor devices (e.g. 68000 series). The character/graphics store 10 may contain one or more sets of characters which may be supplemented from a larger store if desired, e.g. floppy disc.

The manipulation of the image memory address by the system blocks 32 and 33 is shown in more detail in Figure 3. The data and write addresses from processor 36 will be used to give the 625 entries into the manipulation memory 33. Thereafter on read out from the image memory 30 for display, the vertical counter 23 commencing with display line 1, causes address 1 in memory 33 to be accessed and the pixel number stored therein to be entered into incrementer 32. Each pixel clock pulse during line 1 will then increment the pixel number in incrementer 32 as the line is scanned for display. If no manipulation of the image is required, then memory 33 at location 1 would have pixel number 1 previously entered by the operator. Assuming a line length of 702 pixels, then for an unmodified picture, location 2 in memory 33 would have pixel number 703 pre-entered to ensure the next line of the memory 30 is accessed at pixel rate during the next display line, this number being transferred to incrementer 32 during line blanking and thereafter incremented at pixel clock rate during the active line period.

In practice, although sequential locations are accessed to read out location data from memory 33, the sequence of stored pixel numbers therein would not be entered so as to be sequential (e.g. 1, 703, 1405 etc.), if manipulation is required. For example, by loading a descending sequence of addresses into manipulation memory 33 (e.g. .....1405,703,1), the resultant picture would be displayed effectively upside down. The memory 33 requires only a capacity of 625 x 19 bits to handle this manipulation. The address incrementer 32 only requires the capability of handling a single 19 bit word which is incremented at pixel rate and such an incrementer can be fabricated from D type registers. A displayed line need not commence at the first pixel of any given input line. For example location 1 of memory 33 could have pixel number 350 stored therein. This would result in a shift to the left for the displayed picture.

It can then be seen that the system is highly versatile, yet changes can be easily effected. At the most, only 625 entries have to be made to produce a new display configuration, rather than a requirement for 500,000 entries if the operator had to define each pixel in the frame.

As already mentioned, the memory array 30 in practice comprises two memories as now illustrated in Figure 4. Because of this, modification of the arrangement of Figure 2 is required. The memories 40 and 41 are each of sufficient capacity for the operation required and may each be up to a whole frame capacity.

Addressing of frame store 40 may be taken from the processor via source B or from the address incrementer 32 by means of switch 19. Addressing of frame store 41 is taken from address incrementer 32 only.

The operator has access via the keyboard only to frame store 40 and enters data at A at locations defined via B. Once character/graphics composition is completely entered, which will typically take a good number of T.V. frame periods, the data can be transferred in one T.V. frame period to store 41. This transfer is achieved by the address incrementer addressing both store 41 directly and also store 40 via switch 19. Any given address is the read address for store 40 and simultaneously the write address for store 41. Thus, for one complete T.V. frame, the image data is read out of store 40 and written into store 41 under control of the manipulation memory 33 and address incrementer 32, while simultaneously the image data read out of store 40, is passed to the display circuits for display. At the end of one T.V. frame, the image data will have been completely transferred to store 41 and can be read out of store 41 for display of subsequent T.V. frames. Store 40 is then available for updating by the operator.

It should be noted that the passing of the new image data from store 40 via store 41 to the display circuits starts coincident with the start of the transfer process, resulting in minimal delay between the com-

pletion of character/graphics composition in store 40 and commencement of display of the new image data.

Further, due to its relatively small size, the manipulation memory 33 may typically be completely updated in the field blanking interval immediately preceding the start of the transfer process. This allows the new image data to be transferred and displayed with a new sequence of stored pixel numbers, rather than with the old sequence appropriate to the previous image data.

Furthermore, except when transfer of image data is in progress, the operator, via the processor, has sole access to store 40, This allows fast up-dating of the image data compared to interleaved-access memory configurations and, since only one frame store requires modification by the operator and processor, fast up-dating compared to traditional double-buffered memory systems where the two stores are alternately switched between processor and display.

During the T.V. frame for which transfer of image data is in progress, access to store 40 is inhibited, delaying possible up-dating of the image data by the operator. In practice, means is provided for selectively transferring the image data on a T.V. line by line basis. As each new pixel location is read from manipulation memory 33 at the start of each T.V. line, an extra control bit associated with each pixel location is read out to determine whether transfer should occur or not for that line. This control bit can then if necessary inhibit the transfer process for the remainder of the line resulting in the image data being read out of store 41 for that line and allowing processor access to store 40. The control bit associated with each T.V. line may be set or cleared by the operator and processor as required, resulting in image data on only those T.V. lines which require up-dating being transferred. Thus in situations where the whole image is not up-dated at one time, e.g. scrolling, access to the frame store 40 can be made available to the operator and processor except during transfer of those specific lines of image data requiring up-dating. This further provides for fast manipulation and up-dating of image data.

Dynamic effects are achieved by manipulating the read out sequence of store 41 by use of the manipulation memory 33. The write cycle from store 40 to 41 still allows retention of the image in store 40 for selective modification or alternatively replacement by a newly composed image in this store 40. Memory 41 timing can be configured to ensure the read/write cycle can be effected to prevent display data being lost during the single frame transfer period.

The store configuration employed, i.e. where store 40 is always the composing store and store 41 is always the display store ensures cost-effective operation, as any interfacing between the processor 36 and the memory is not duplicated nor is there a requirement for complicated switching of store 40 and 41 input/output between the graphics input and display.

In the Figure 5 embodiment, the system has been modified whereby the manipulation memory 33 of Figure 4 is incorporated into the frame stores 40 and 41. The memory capacity of stores 40 and 41 is chosen to be sufficiently large to store the extra manipulation data which is equivalent to a few t.v. lines of data. Entries of 625 x 19 bits typically require just under 3 lines of storage, each location of 8 bit capacity, assuming approximately 700 storage locations per line. During normal display, image data from store 41 is read out under control of the manipulation data also held in store 41.

The frame stores do not discriminate between manipulation data and image data. To read the first portion of manipulation data into the address incrementer 32, the vertical counter 50, during blanking before line 1, will produce an address via switch 51 corresponding to the first store address to allow the 19 bit word to be read out and held by incrementer 32. This is used via switch 51 to define the line of image data read out and the addresses are incremented at pixel rate during the active line period. During line blanking prior to line 2 the incremented counter 50 produces a second address to allow the next 19 bit manipulation address to be entered from store 33 into incrementer 32.

During the second line period, this new address is incremented pixel by pixel. Thus each manipulator word is read out line by line for use during each of the active line periods.

Character/graphics data may be composed or updated in store 40 by the operator and processor and in addition, a new sequence of stored pixel numbers pertaining to the new image may be entered into the manipulation data area of store 40.

Transfer of the new image data and of the manipulation data to store 41 then occurs over 1 T.V. frame period, under control of the manipulation data in store 40, by means of the simultaneous read/write transfer process already described. Note that there is now no necessity to up-date the manipulation data in the field blanking interval prior to the transfer process, since as each manipulation address is read out of store 40 at the start of each line for entry into incrementer 32 it is simultaneously written into the manipulation data area of store 41. Thus after one T.V. frame the complete manipulation data will have been transferred in addition to the desired number of lines of image data.

In view of the standard RAM addressing techniques for video access rates, where 8 pixels are accessed for a single pixel address, 8 pixels are available for one readout as shown in Figure 6. Each pixel location holds 8 bits of data, so that if 3 of these pixel locations are actually used for storing one manipulator address this will allow a word length of 24 bits to be available, which is more than sufficient for the 19 bit word requirement.

Although in the examples a frame of 625 lines has been discussed, in practice only about 576 are active display lines, so even if the frame store is chosen with only a 625 line capacity, some of these lines of the frame could in practice be employed for the manipulation store. The addressing structure would be adjusted accordingly.

Where only a portion of the display is always intended to carry graphics/character information the store requirements can be further reduced.

The use of a single store for both the manipulation data and the image data reduces interfacing to the processor and minimises complexity and cost.

Although the configurations above have been described in terms of manually entering each manipulator address value, in practice pre-entered routines in the processor could be selected to automatically calculate these values for a given effect.

The embodiments described allow the relatively slow software control of the manipulator memory to be adequate to cope with the video display rates yet allow a variety of dynamic effects to be achieved.

Some of the possibilities are as follows:-

1. By clearing one raster line of the main memory array and then setting all manipulation memory values to that line the entire display may be instantly cleared.

2. By loading a descending sequence by raster line addresses into the manipulation memory the picture may be displayed upside down.

3. Memory areas longer than the normal raster line may be set up to permit the crawling of text from left to right, the dynamic movement being created by incrementing a group of manipulation addresses on a field by field basis.

4. By progressively filling the manipulation memory with valid address on a field by field basis a picture may be wiped onto the screen.

5. In devices such as character generators a percentage of t.v. lines can always be guaranteed to be blank, i.e. areas between rows of text. However, the blank lines will vary in position on the screen from caption to caption. Where such a redundancy can be guaranteed this technique can take advantage of this by using a smaller memory array. In the case of specialist applications such as sports timing displays only perhaps 10% of the lines on the screen will be required in any give caption yielding a very useful saving in cost. Conversely it is possible to use a very much larger memory array to achieve more complex effects. If the memory array were twice that required to fill a screen then effects such as wiping between pictures and displacing one picture to reveal another could be implemented.

Although the preferred arrangement described employs two frame stores and permits a new frame to be set up in one store whilst the other is being displayed, it will be appreciated that if this feature is not required then the store 41 could be dispensed with. In such an arrangement the output of the single frame store 40 could be arranged to be blocked until the frame is fully updated. Such an arrangement is considered to fall within the scope of this invention.

CLAIMS

1. A manipulation system comprising a character/graphics generator, a video memory for storing data provided by the character/graphics generator, a manipulation memory for holding selected address parameters pertaining to individual displayed video lines defining the start addresses of picture information read out from the video memory and means for incrementing or decrementing video memory addresses commencing from the start address available from the manipulation memory to allow data from the video memory to be read out in a manipulated sequence.

2. A manipulation system as claimed in claim 1, wherein the manipulation memory forms part of the video memory.

3. A manipulation system as claimed in claim 1 or 2, comprising a processor responsive to command information for selectively routing a character/graphic for storage by the video memory at a defined address.

4. A manipulation system as claimed in claim 1, 2 or 3, wherein the manipulation memory has a capacity which permits storage of an address of each line of a video display.

5. A manipulation system as claimed in claim 4, wherein the means for incrementing or decrementing the video memory address is coupled with a timing arrangement which provides input pulses corresponding to the line frequency of the display and clock pulses corresponding to incremental steps from the start of the line.

6. A manipulation system as claimed in claim 5, including a vertical counter coupled with the timing arrangement to receive the line frequency pulses and field flyback pulses, which vertical counter is coupled with the manipulation memory to increment or decrement the video memory address at each flyback pulse.

7. A manipulation system as claimed in claim 6, including switch means between the manipulation memory, the vertical counter and the command source for permitting selective updating of the manipulation memory.

8. A manipulation system as claimed in any one of the preceding claims, wherein the video memory comprises first and second video stores for storing data indirectly and/or directly provided by the character/graphics generator.

9. A manipulation system as claimed in claim 8, wherein each video store has a capacity of at least one frame of video information.

10. A manipulation system as claimed in claim 8 or 9, wherein only the first video store is arranged to receive character/graphics data from the generator and thereafter to rapidly transfer the composed image to the second video memory for display.

11. A manipulation system as claimed in any one of claims 8 to 10, wherein the second video store is available for read out during updating of the first video store and means is provided for inhibiting updating access to the first store during transfer of stored data from the first to the second store.

12. A manipulation system as claimed in any one of claims 8 to 10, wherein means is provided for selectively transferring image data from the first video store to the second video store on a line by line basis.

13. A manipulation system as claimed in claim 12, wherein an additional bit is included in the video information at the start of each line to indicate whether that line has been updated, which bit is effective to inhibit the transfer of that line between first and second video stores, to effect retention in the second video store of existing stored information and permit access to the memory location in the first video store for immediate updating.

14. A manipulation system as claimed in claim 13,

wherein means is provided whereby the additional control bit may be set or cleared by an operator.

15. A manipulation system substantially as described herein with reference to Figures 2 to 6 of the drawings.

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